ABSTRACT OF THE DISCLOSURE

The invention relates to a component with a large grain dynamically reconfigurable architecture for processing of data by processing units organized in rows and connected to each other through interconnections so as to enable processing in pipeline or parallel mode or in dependent rows mode. All data types may be processed and the component may process several applications at the same time. The choice of the grain, control at several levels with limited control interconnection resources and the data distribution circuit enable local or general reconfiguration of the component in one clock cycle.